Advanced FPGA-based System Designing Laboratory

Innovation Professionalism Brainstorming Enthusiasm

Why do we stand apart?

This lab is being molded into the first one, at EE Department at UET Lahore, to be developed around a true industry-academia relationship boasting a prosperous R&D environment

Courses that avail the facilities offered by the lab:

Undergraduate Courses:

- Digital Logic Design
- Microprocessor Systems
- Computer Architecture

Postgraduate Courses:

- Advanced Computer Architecture
- Embedded Engineering
- FPGA/ASIC Design

Digital Logic Design:

Students start from basic combinational and sequential system design by interconnecting various logic chips to create subsystems and systems. Afterwards they are taught fundamentals of RTL design using Verilog. They are made to understand elementary concepts regarding logic synthesis and verification. Towards the end of the semester students are supposed to develop Verilog codes for the subsystems they initially hardwired in the lab. These synthesizable projects are then tested and verified on CPLDs and FPGAs. This lends them a preliminary idea of IP core development for the domain of Reconfigurable Logic.

Computer Architecture:

The lab kicks off with a Verilog refresher and students move on to learn advanced RTL design and digital system verification. They are taught system design using the "Data Path and Control" paradigm. This laboratory workload has been designed in an effort to assist the theory class where students are taught RISC Machine Design through text authored by Hennessey and Patterson. The lab work revolves around students developing single-cycle and multi-cycle RISC machines. The waveforms generated using test-benches aid students in a better understanding of the RISC machine operation and hence a proper idea of processor operation.

Later on the students are supposed to modify both the Data Path and the Control in order to incorporate a larger set of instructions.

The students also get hands on experience of core development of I/O interfaces by developing a standard digital communications protocol project e.g. the RS232. This gives them a handy idea of underlying theory of digital buses and I/O communications.

The last portion of the lab becomes pretty exciting when students generate custom IP cores of the Microblaze processor provided by Xilinx Inc. Students get to create and operate their own custom processors on FPGAs and later on debug code segments on it giving them a rather through idea of microprocessor based system development. After enduring the rigor of this lab and its predecessor, students become enough well-trained to enter with confidence into the Reconfigurable Logic Industry as they have had been trained on the state-of the-art tools and technology.

Embedded Engineering:

This course introduces students to microcontrollers/microprocessors ranging from 8-bit to 32-bit architectures. This course is about the efficacy and on the integration of such devices in modern day embedded systems for control and automation.

A part of the course revolves around utilizing Real Time Operating System kernels for tedious embedded systems control and data processing scenarios. Students are exposed to RTOS kernels in the limelight of Nucleus/uCOS kernels. As a part of practical experience regarding RTOS integrated embedded system development, students employ basic RTOS concepts in applications developed on PowerPC and Microblaze microprocessor IP cores (which are configured and operated on the Field programmable devices).

FPGA/ASIC Design:

This course is a dedicated to state-of-the-art system development on FPGAs. Here the students move on from Verilog to the more structured VHDL for system description purposes. The course emphasizes on System on Chip development (SoC).

Laboratory work focuses on implementation of concepts studied in the theory class. A portion of the laboratory gives special detailed treatment to Sequential Control Unit design for Reconfigurable Logic.

As far as Data Path development is concerned, students build parallel/semi-parallel algorithms and architectures for various types of data processing related to real time digital signal processing e.g. the FFT and FIR/IIR filter structures. Special treatment is given to numerical techniques for matrix algebra by developing Systolic architectures and hardware algorithms for solving these arithmetic problems. After

synthesizing their systems, students develop an in-depth understanding of time/area tradeoffs encountered in system development on Field Programmable Gate Arrays. All this understanding owes to the time/area analysis encountered during synthesis of parallel and semi-parallel architecture design for SoC.

Students later on code a synthesizable core for a mini-RISC machine and test and verify it on FPGAs. To teach IP core integration and development, students are either made to integrate an I/O peripheral with this mini-RISC machine.

In the ends students get a healthy exposure to Hardware-Software Co-Design by developing a system (which incorporates the customizable Microblaze processor and a set of dedicated MAC blocks) for an adaptive filtering problem, where the weight update algorithm is designed in software.

Summer Courses and Internships:

Both undergraduate and graduate students are offered short courses (ranging from 2-4 weeks) on:

- Synthesizable HDL coding techniques for FPGAs
- Data Path and Control Design for Algorithms
- DSP for FPGAs
  - Algorithms and Architectures for DSP
  - CORDIC Processing and Distributed Arithmetic
- Fundamentals of RTOS
- Utilizing the Microblaze and PowerPC IP cores

This lab also provides undergraduate senior year students with an opportunity for internships during summers. Students learn and afterwards assist in devising, analyzing and eventually implementing semi-parallel and parallel architectures for various computationally expensive algorithms.

Research and Development Activities:

- **A Paradigm for Evaluation of Linear Matrix Algebra on Reconfigurable Logic:**

  This project is about formalizing a generalized approach towards developing systems based upon recursive matrix algebra. A paradigm, following whose approach, will lead towards design of systems which incorporates algorithms for MIMO and Adaptive Control systems (e.g. the Kalman Filter and the H-Infinity filter).

  First phase of system development has been completed. This included the development of parallel architectures for linear matrix algebra numerical techniques (LU Decomposition, Triangular Matrix Inversion etc.) and overall local and global control of the data path developed. The unique aspect of the design was that all the architectures output the result for an 'NxN' input

matrix in 'N' clock cycles with utilizing no more than 'N^2' data processing elements.

The second phase is focused towards mapping of these architectures onto each other so that no more than 'N^2' will be able to perform various algorithmic computations. Moreover, local memories are being incorporated into the architecture so a healthy number of matrices may reside within the array, thereby reducing data I/O complexity to and from the arrays. Also a unique hierarchical control is being developed for such complex data path.

- **Systems and Architectures for Harmonic Analysis on Reconfigurable Logic:**

  We have thoroughly surveyed existing techniques encompassing architectures for Harmonic Analysis (DFT, FFT and AFT). Now we are in the process of devising hardware algorithms which carefully exploit expensive reconfigurable logic area and resources.

  We are coming to terms with development of parallel and semi-parallel systems for these algorithms with a perspective towards design targeting the individual hard and soft real time constraints of each particular application. Applications range from speech processing, software defined radio (SDR) and codec design to power line/systems harmonic analysis and biomedical signal analysis. This project concerns with analysis of throughput of transformed data, clock speed of the developed architectures, and the logic resources utilization and power consumption of these systems on reconfigurable devices.

- **HW/SW Co-Design for Adaptive Control Algorithms:**

  This project has recently been started and is about Adaptive Filter development on FPGAs using Hardware Software Co-Design. Strategy that is to be employed is to develop fully parallel pipelined filter structures but the filter coefficients or, as in our case, adaptive weights are to be computed using soft-processing or more precisely using a microprocessor core. Later on, an analysis will be made on suitability of division into hardware and software of various portions of the adaptive filter class of algorithms (Kalman, LMS, RLS etc.).

- **Memory based Systems for Solution of Graph Theory Algorithms pertaining DNA Sequencing:**

  This idea is rather in its nascence and is about a system of a hierarchy of dedicated memories whose sole purpose is to facilitate the solution of graph theory algorithms. The unique concept is that, without microprocessor intervention (which we can justify will result in redundant data manipulations), algorithms will be solved with the help of multiple tiny hardware accelerators. The trick in this project lies around arranging data acquired from DNA strands into fixed data formats and then manipulating these fixed data formats (residing in the hierarchy of memories) to achieve solutions for these algorithms.

Selected Publications:

- M. A. Jamil, Dr. Zubair Ahmad Khan **"Design and Development of Communication Adapter for Legacy Substation Devices"** ICEE 2007, 11-12 APRIL 2007.

- K.Anwar, Z.A.Khan **"Dynamic Priority Based Message on Controller Area Network"** ICEE 2007, 11-12 APRIL 2007.

- Taha Sajjad, Dr. Zubair Ahmed Khan **"Comparison of Speech Response of Normal Hearing Listener and Cochlear Implanted Patient using Model for Chaotic System"** INMIC 2007, 28-30 December 2007.

- M. Akbar, Z. A. Khan **"Modified Nonintrusive Appliance Load Monitoring For Nonlinear Devices"** INMIC 2007, 28-30 December 2007.

- Ali Faisal Murtaza, Z A khan, " **Starvation Free Controller Area Network using Master Node**" ICEE 2008, 25-26 March 2008.

- *Taha Sajjad and Zubair Ahmad Khan,* **"Identification Speech Response of Cochlear Implant Patient using Chaotic Model"** ICEE 2008, 25-26 March 2008.

- K.Anwar, Z A Khan **"On Simulating Dynamic Priorities in Controller Area Network"** IBCAST 2008, 2008.

- Fahad Ahmad Khan, Rizwan Arshad Ashraf, Qammar Hussain Abbasi, Ali Arshad Nasir, **"Resource Efficient Parallel Architectures for Linear Matrix Algebra in Real Time Adaptive Control Algorithms on Reconfigurable Logic"**, ICEE 2008, 25-26 March 2008.

Resources and Equipment:

Xilinx ISE 7.1 (Registered Version), Xilinx EDK 7.1 (Registered Version)

Xilinx ISE 8.2 (Registered Version), Xilinx EDK 8.2 (Registered Version)

ModelSim 6.0 (Evaluation Version)

Chipscope Pro (Evaluation Version)

Nucleus RTOS Tools for EDK 7.1 (Evaluation Version)

Nucleus RTOS Tools for EDK 8.2 (Evaluation Version)

Spatan 3 Starter Kits, Spartan 3E Starter Kits

Virtex Development Boards

Agilent Technologies Logic Analyzer

Courses Affiliated with the Laboratory
UNDERGRADUATE COURSES

Course No. EE131
Course Title DIGITAL LOGIC DESIGN
Credit Hours 3+1

Course No. EE430
Course Title COMPUTER ARCHITECTURE AND DESIGN
Credit Hours 3 + 1

Course No. EE330
Course Title MICROPROCESSOR SYSTEMS
Credit Hours 3+1

GRADUATE COURSES

Course No.EE 510
Course Title: FPGA/ASIC Design
Credit Units: 3.0
Course Type: Elective

Course No.: EE 650
Course Title: VLSI System Design
Credit Units: 1.0
Course Type: Elective

Course No.: EE651
Course Title: Advanced Computer Architecture
Credit Units: 1.0
Course Type: Elective

Course No.: EE 667
Course Title: Embedded Engineering
Credit Units: 1.0
Course Type: Elective

PROPOSED GRADUATE COURSES

Course No.: EE 5xx
Course Title: Verilog HDL: Modeling, Simulation, and Synthesis
Credit Units: 3.0
Course Type: Elective

Course No.:EE 5xx
Course Title: Application Specific Integrated Circuit Development
Credit Units: 3.0
Course Type: Elective